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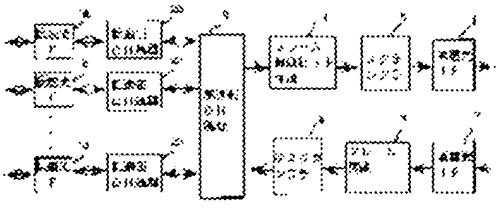
(54) SDH TRANSMISSION SYSTEM

(57)Abstract:

PURPOSE: To prevent the generation of a long fixed pattern by keeping the only one part of a frame synchronizing pattern unscrambled and scrambling the other long bits.



CONSTITUTION: A low-speed overhead processing section 2 multiples signals from a low-speed optical interface 1 and the signal is processed by a high-speed overhead processing section 3. A frame synchronizing pattern addition section 4 adds frame synchronizing patterns and a scrambler 5 scrambles the area (total 4 bytes) including an A1 in 2 bytes and A2 in 2 bytes and all bits excluding 3×64 bytes followed by C1 byte. Further, it is transmitted through a high- speed optical interface 6. Signals received through a high-speed optical interface 7 is synchronized at a frame synchronizing section 8 by using the unscrambled A1+A2 byte of 4 bytes, periodically resetting a scrambler 9.

LEGAL STATUS

[Date of request for examination]

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[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The SDH transmission system characterized by transmitting to all the bits except some frame synchro patterns in the SDH (Synchronous Digital Hierarchy) transmission frame of G.CCITT advice 708 convention, applying a scrambler.
[Claim 2] The SDH transmission system characterized by transmitting to all the bits except the reservation field of the proper application of each country following some frame synchro patterns, a multiplex number, and it in an SDH transmission frame, applying a scrambler.
[Claim 3] The part which is not scrambled in claims 1 or 2 is an SDH transmission system characterized by being the field which contains A1 of G.CCITT advice 708 convention, and A2 byte continuously.
[Claim 4] The part which is not scrambled in claim 3 is an SDH transmission system characterized by being the continuous field which contains 2 bytes and 2 bytes of A2 for A1.
[Claim 5] It is the SDH transmission system characterized by being the pattern which reverses a frame synchro pattern A1 and A2 pattern for every byte in the SDH (Synchronous Digital Hierarchy) transmission frame of G.CCITT advice 708 convention.
[Claim 6] Using the bit string of G.708 convention for some frame synchro patterns in the SDH (Synchronous Digital Hierarchy) transmission frame of G.CCITT advice 708 convention, other frame synchro patterns aré '1010... It is the SDH transmission system characterized by being 'pattern.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the transmission system which uses an SDH (Synchronous Digital Hierarchy) transmission frame.
[0002]
[Description of the Prior Art] The conventional SDH transmission frame structure is shown in drawing 2 . Except for the reservation field for the frame synchro pattern called A1 byte and A2 byte in a STM-n frame, the identification number of the signal which is called 1 byte of C following it and which is multiplexed, and the application of the proper of each country which follows it further, and a total of nine xn bytes, the scramble is applied to all transmitted bits so that the CCITT advice G.708-709 may set.
[0003]
[Problem(s) to be Solved by the Invention] It is transmitted in the above-mentioned conventional technique, without scrambling A1, A2, 1 byte of C, and a total of nine xn bytes of reservation field continuously about multiplex [of 155Mbps units / several n]. The bit length of the fixed pattern which is not scrambled becomes long as n increases here (i.e., as transmission speed becomes quick). about [for example, / which is called STM-64] -- in the transmission system of 10G bit per second, A1, A2, 1 byte of long C, and the long reservation field which amount to 576 bytes will be transmitted as a fixed pattern on a transmission line -- it divides and comes out. In the transmission system using an NRZ code, although it has defined that the CCITT advice G.957 uses an NRZ code for the transmission-line sign of an SDH transmission system, when a long fixed pattern appears periodically, a big pattern jitter and a big intersymbol interference may be produced, and it may become the factor which worsens a bit error rate. Although bit string'11110110' is used for a frame synchro pattern A1 and bit string'00101000' is used for A2 especially conventionally, since each pattern has not taken the direct-current balance, it has risk of a dc component being intercepted and leading to big wave degradation in the receiving circuit by AC association used well conventionally.
[0004] Here, if a scramble is applied to all bits also including a frame synchro pattern, although the above-mentioned trouble is solved, a new problem will produce it. If a receiver does not descramble received data, it becomes impossible in this case, to identify a frame synchro pattern. It is difficult for the descrambler to operate by applying reset with a transmission frame period, and to operate a descrambler correctly, without taking frame synchronization. Therefore, when the scramble was applied to all bits, there was a problem that a receiver could not receive data correctly.
[0005]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, it leaves some frame synchro patterns, without applying a scramble, and the approach to which a scramble is applied is effective in other long bits. Since especially the approach only the field (a total of 4 bytes) which contains 2 bytes and 2 bytes of A2 continuously does not scramble A1 contains in division into equal parts a different bit pattern called A1 and A2, it has the advantage from which the frame incorrect

synchronization of a 1-byte gap cannot arise easily.
[0006] The method of choosing a pattern different from the former as a non-scrambling cutting tool as another solution means is also effective. For example, when a frame synchro pattern A1 and A2 pattern are used as the pattern reversed for every byte, they have the advantage which cannot receive wave degradation by direct-current cutoff of a receiver easily. Moreover, only die length required for frame synchronization uses conventional A1 and an A2 byte pattern, and it is '1010 to other fields... A direct-current balance like 'pattern can be taken, and the approach using the small pattern of a pattern jitter is also effective.
[0007]
[Function] Generating of a long fixed pattern can be prevented like **** by leaving some frame synchro patterns, without applying a scramble, and applying a scramble to other long bits. Since the probability that a direct-current balance can be taken by scramble in the fixed section is high, generating of a pattern jitter or an intersymbol interference can be suppressed.
[0008] Moreover, the method of have taken the direct-current balance different from the former to the non-scrambling cutting tool, and choosing the small pattern of a pattern jitter is also effective by the same reason.
[0009]
[Example] Explanation of the example of this invention is given using drawing 1 . Drawing 1 is drawing showing one example of this invention applied to STM-64, and illustrates only the part of the section overhead of STM-64 transmission frame given in drawing 2 . In STM-64 frame, data are transmitted by making the reservation field for the frame synchro pattern called A1 byte and A2 byte, the identification number of the signal which is called 1 byte of C following it and which is multiplexed, and the application of the proper of each country which follows it further, and a total of nine x64 bytes into a head so that the CCITT advice G.708-709 may set. In this example, a scramble is not applied only to 3x64 bytes following the field (a total of 4 bytes) and 1 byte of C which contain 2 bytes and 2 bytes of A2 for A1 continuously.
[0010] Since this approach contains in division into equal parts a different bit pattern called A1 and A2, it is the optimal in the alternative which the frame incorrect synchronization of a 1-byte gap cannot take place easily, and chooses the non-scrambling field which is 4 bytes. Moreover, if the non-scrambling section is made into 3x64 bytes following A1 byte 64 byte, A2 byte 64 byte, and 1 byte of C, although a little long fixed pattern will appear, frame synchronization can be independently taken by 64 low-speed signals.
[0011] The configuration at the time of applying the 1st example to an asynchronous transfer mode device at drawing 3 was shown. An asynchronous transfer mode device consists of the low-speed optical interface 1, the low-speed section overhead processing section 2, the high-speed section overhead processing section 3, the frame synchro pattern adjunct 4, a scrambler 5, high-speed optical interfaces 6 and 7, the frame synchronization section 8, and a descrambler 9. The signal from the low-speed optical interface 1 is processed and multiplexed in the low-speed section overhead processing section 2, and is processed in the high-speed section overhead processing section 3, and after a frame synchro pattern is added by the frame synchro pattern adjunct 4, a scramble is applied to all the bits except 3x64 bytes following the field (a total of 4 bytes) and 1 byte of C which contain [5] 2 bytes and 2 bytes of A2 for a scramblerA1 continuously. Furthermore, it is transmitted through the high-speed optical interface 6. Moreover, using 4 bytes the A1+A2 byte which a scramble has not required, the signal received through the high-speed optical interface 7 takes a synchronization in the frame synchronization section 8, and descrambles correctly by resetting a descrambler 9 periodically using a frame signal. Furthermore, it is processed through the high-speed section overhead processing section 3 and the low-speed section overhead processing section 2, and is transmitted from the low-speed optical interface 1.
[0012] It is obtained by five steps of forward alignment guard time, and, as for a frame synchronization property, the engine performance of incorrect synchronous level of significance and 1% or less of re-hunting level of significance will be obtained by two steps of backward alignment guard time average mistake frame spacing ten years by using 4 bytes of frame synchro pattern. The frame synchronization

circuit of five steps of front and two steps of back is the range easily realizable by 1LSI.
[0013] Moreover, another configuration at the time of applying the 1st example to an asynchronous transfer mode device was shown in drawing 4 . It is the description that do not have the high-speed section overhead processing section 3 in this example of application, but only the number of low-speed optical interfaces has the frame synchro pattern adjunct 4, a scrambler 5, the frame synchronization section 8, and a descrambler 9. Here, only a cutting tool synchronization is taken [10] using the cutting tool synchronizerA1 and A2 byte, it decomposes into 64 STM-1 signals using 1 byte of C which is not scrambled too, and signal processing of frame synchronization, descrambling, and others is performed per STM-1 signal after that. The data similarly assembled in the low-speed section are transmitted from the high-speed optical interface 6 only by multiplex being carried out in the multiplex section 11.
[0014] The 2nd example of this invention is shown in drawing 5 . The frame synchro pattern A1 and A2 pattern are used as the pattern reversed for every byte. For this reason, there is an advantage which cannot receive wave degradation by direct-current cutoff of a receiver easily.
[0015] Furthermore, as other examples, only die length required for frame synchronization uses conventional A1 and an A2 byte pattern, and it is '1010 to other fields... A direct-current balance like 'pattern can be taken, and the approach using the small pattern of a pattern jitter is also effective.
[0016]
[Effect of the Invention] By this invention, a long fixed pattern is not generated in ultra high-speed transmission using an SDH transmission frame. Even if this uses a simple circuit for identification, a timing extract circuit, etc. in ultra high-speed transmission using an SDH transmission frame, a stable transmission system with small jitter and intersymbol interference is realizable.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing one example of this invention applied to STM-64
[Drawing 2] Drawing showing the frame structure of STM-64
[Drawing 3] Drawing showing the example of application to the asynchronous transfer mode device of this invention
[Drawing 4] Drawing showing another example of application to the asynchronous transfer mode device of this invention
[Drawing 5] Drawing showing another example of this invention applied to STM-64
[Description of Notations]
1 A low-speed optical interface, 2 The low-speed section overhead processing section, 3 The high-speed section overhead processing section, 4 A frame synchro pattern adjunct, 5 A scrambler, 6 A high-speed optical interface, 7 High-speed optical interface 8 The frame synchronization section, 9 Descrambler 10 A cutting tool synchronizer, 11 Multiplex section.

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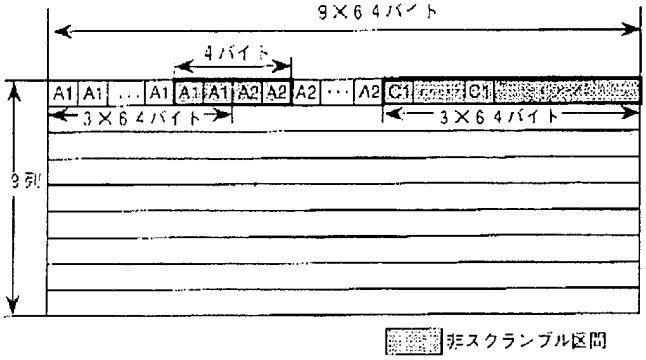
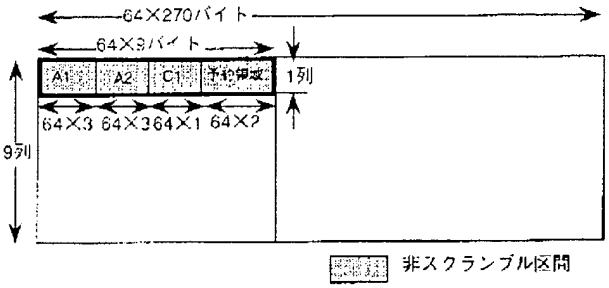
DRAWINGS

[Drawing 1]
(図1)

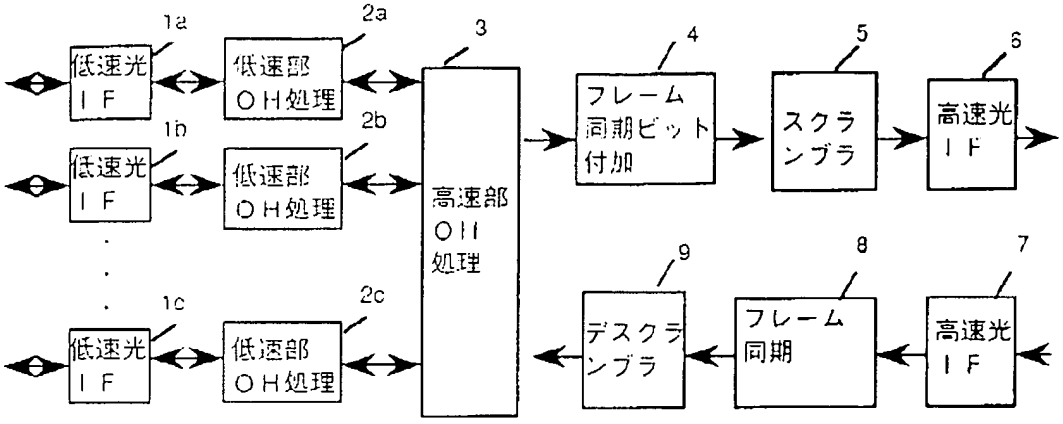


[Drawing 2]
(図2)

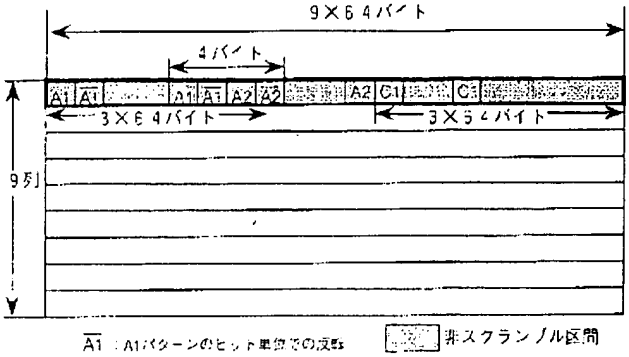


[Drawing 3]

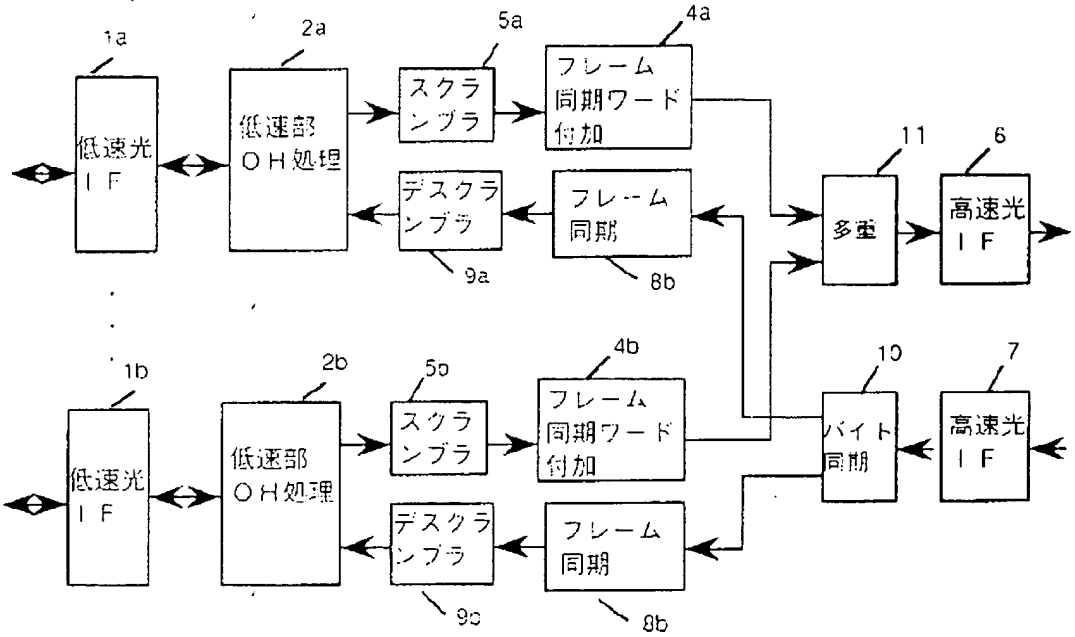
（図３）



[Drawing 5]
(図5)



[Drawing 4]
（図４）



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